**Lab 7**

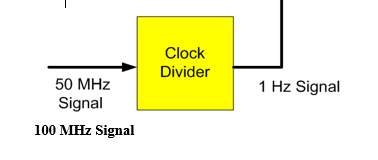
**Implementation of a 3 bit up and down counter using FPGA’s source clock and Clock Divider**

**Objective:**

* To become familiarized with behavior level modeling
* To be able to implement sequential circuits using Verilog
* To implement a 3 Bit Up and Down Counter on Spartan 6 FPGA starter kit.

**Block Diagram:** The Spartan 6 kit has a clock source of 100 Mhz. If we use it in applications like counters, the counter will count at an incredibly fast speed and we will not be able to see the output. Your task is to divide the 100 MHz frequency into a 1 Hz frequency. The Module Clock divider is responsible will be responsible for it.

The functional detail of the 8-bit Ring Counter is shown in the following figures.



**I/O Connection:**

The output of the Counter should be connected to 7 segment display on Spartan 6 Starter Kit. The clock input is connected to pin “V10” on the board. The next number should show with an interval of 1 second.

1-Implement 3 bit Up Counter using FPGA’s clock source and clock divider

2-Implement 3-bit Down Counter using FPGA’s clock source and clock divider

3- Implement 3-bit Up and Down Counter using RST if the RST is high it should Count Up if it is low it should Count Down and display the count in the seven segment display.

4-Implement Lab 6 using FPGA’s clock source.